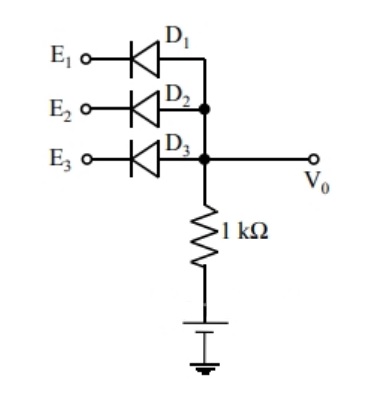
Computer Organization and Architecture

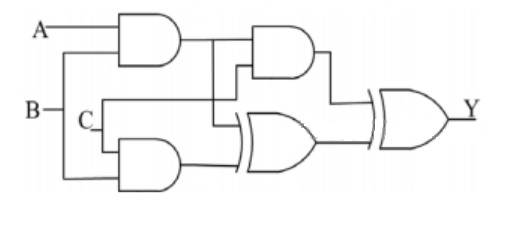
Assignment 1

Answer the following with detailed solution:

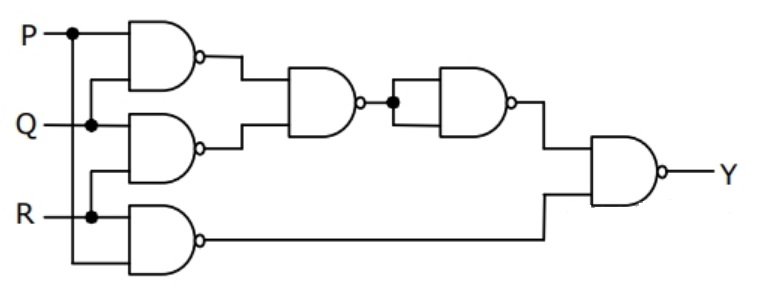
1. The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is
2. 4
3. 5
4. 6
5. 7
6. In the circuit shown, diodes and are ideal, and the inputs and are “0 V” for logic ‘0’ and “10 V” for logic ‘1’. What logic gate does the circuit represent?



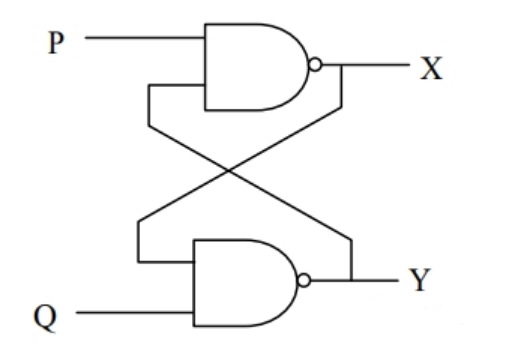
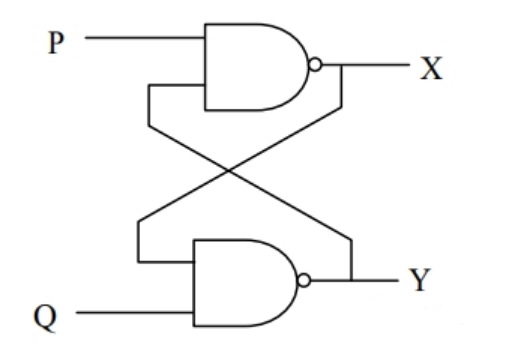
1. 3-input OR gate
2. 3-input NOR gate
3. 3-input AND gate
4. 3-input XOR gate
5. The output of the combinational circuit given below is:



1. A+B+C
2. A(B+C)
3. B(+A)
4. C(A+B)
5. A bulb in a staircase has two switches, one switch being on the ground floor and the other one on the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches, irrespective of the state of the other switch. The logic of switching of the bulb resembles.
6. An AND gate
7. An OR gate
8. An XOR gate
9. A NAND gate
10. The output Y in the circuit below is always ‘1’ when



1. Two or more of the inputs P, Q, R are ‘0’
2. Two or more of the inputs P, Q, R are ‘1’
3. Any odd number of the inputs P, Q, R is ‘0’
4. Any odd number of the inputs P, Q, R is ‘1’
5. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is: P = Q = “0‟. If the input condition is changed simultaneously to P = Q = “1”, the outputs X and Y are



1. X = ‘1’, Y =’1’
2. Either X = ‘1’, Y = ‘0’ or X =’0’, Y = ‘1’
3. Either X = ‘1’, Y = ‘1’ or X =’0’, Y = ‘0’
4. X = ‘0’, Y =’0’
5. Multiply (-10) and (-4) using Booth's algorithm.
6. Multiply (-15) and (-12) using Booth's algorithm.
7. Multiply (5) and (-4) using Booth's algorithm.
8. Multiply (-15) and (4) using Booth's algorithm.
9. Divide (-124) and (-2) using 2’s compliment method.
10. Divide (-125) and (-2) using 2’s compliment method.